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MS-7129 **IBM Wellfleet Next Generation**

Version 0A

Intel (R) Grantsdale (GMCH) + ICH6 Chipset
Intel Tejas & Prescott LGA775 Processor

CPU:

Intel Tejas & Prescott - 3.8G

System Chipset:

Intel (R) Grantsdale (GMCH) North Bridge
Intel (R) ICH6 South Bridge

On Board Chipset:

BIOS -- FWH 4M EEPROM
AC'97 Codec -- AD1981B
LPC Super I/O -- NS PC8374L/K/T
LAN -- BCM 4401/5702/5705M LAN
CLOCK -- ICS954101DF

Main Memory:


2 CHANNEL DDR2 * 2 (Max 2GB)

PCI-E Slots:

PCI-E X1 & PCI & ADD2-N SLOT

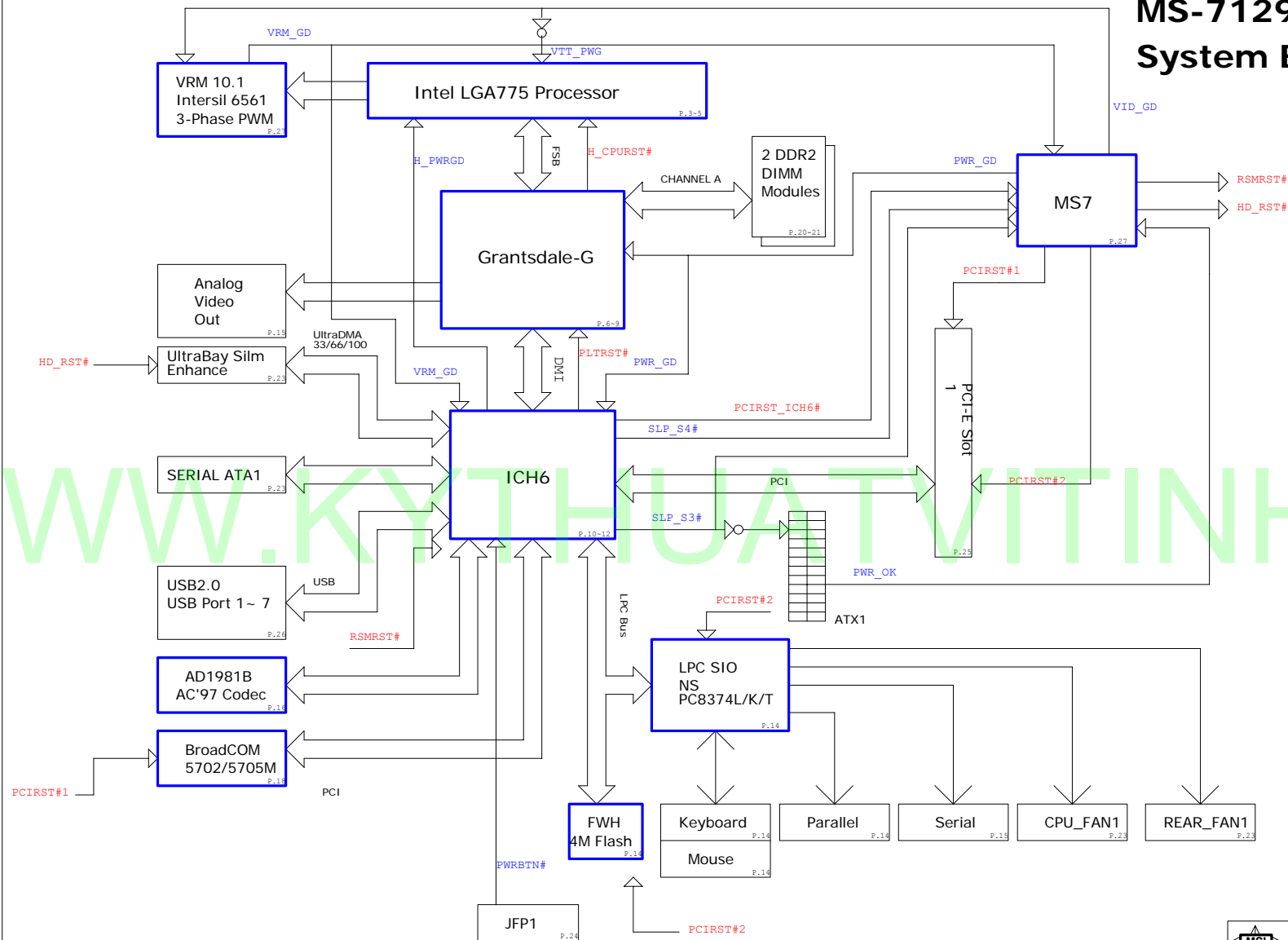
Intersil PWM:

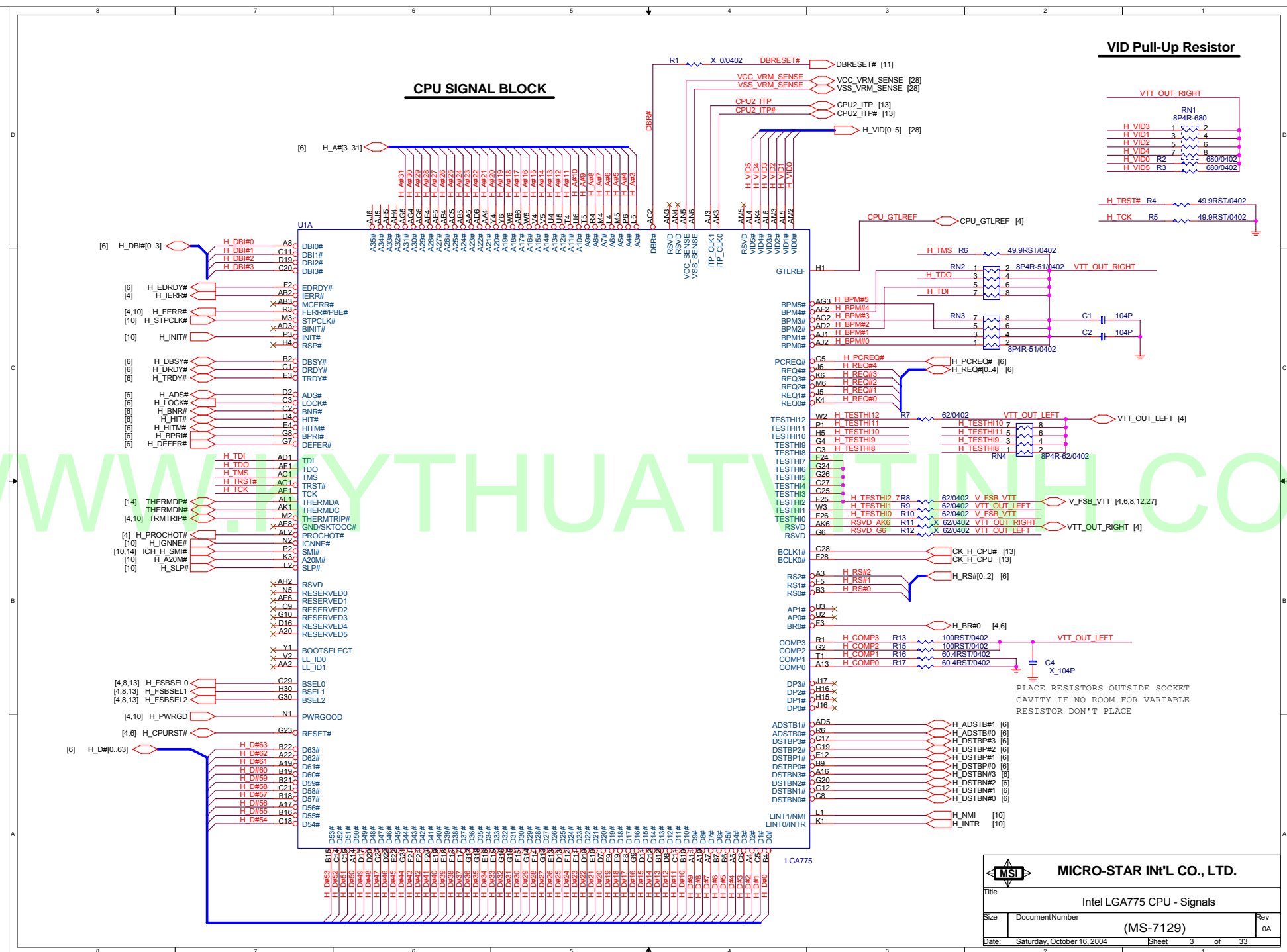
Controller: HIP6565ACV
Driver: HIP6602B *1 / HIP6601B * 1

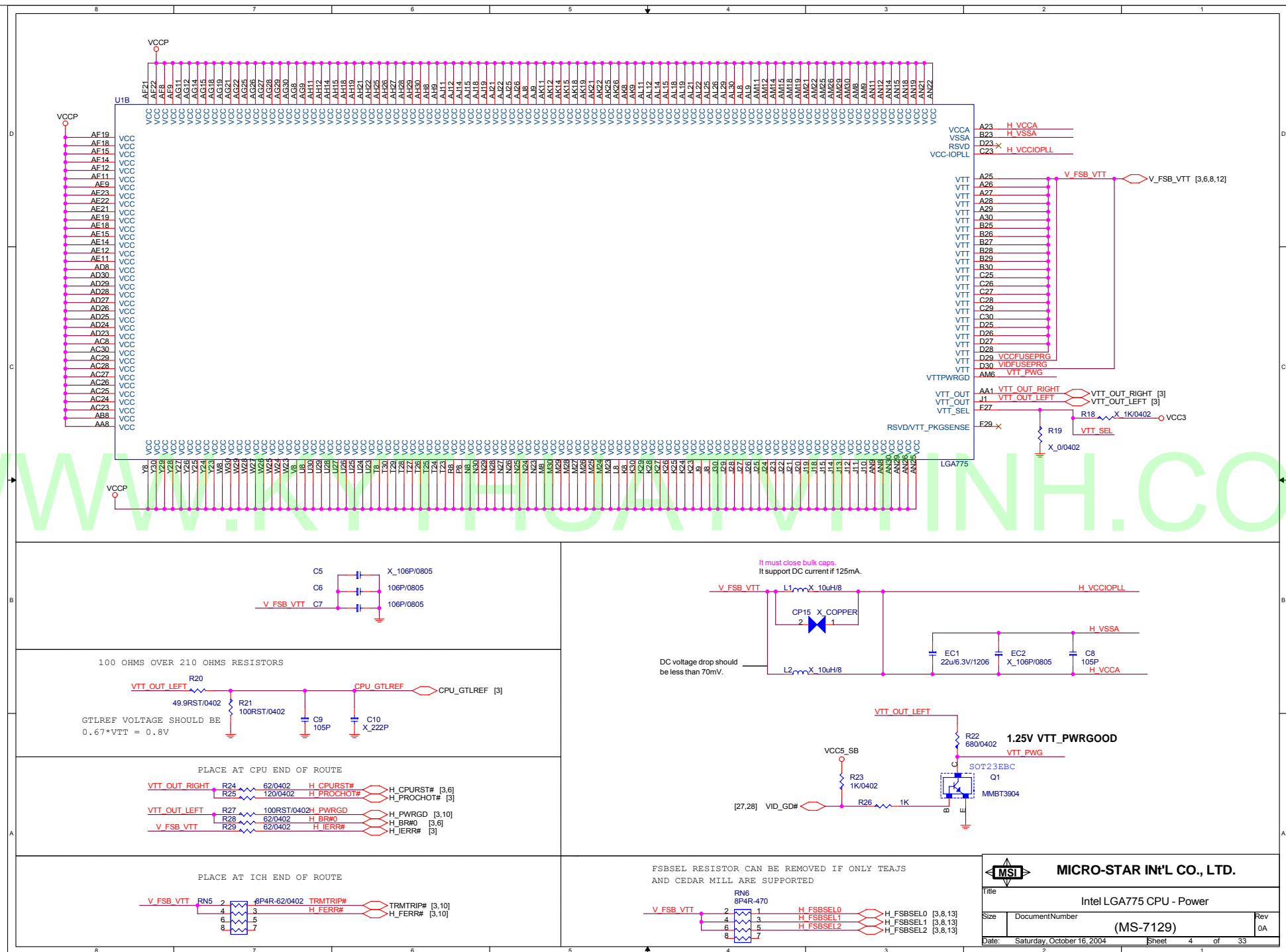
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Title: COVER SHEET			
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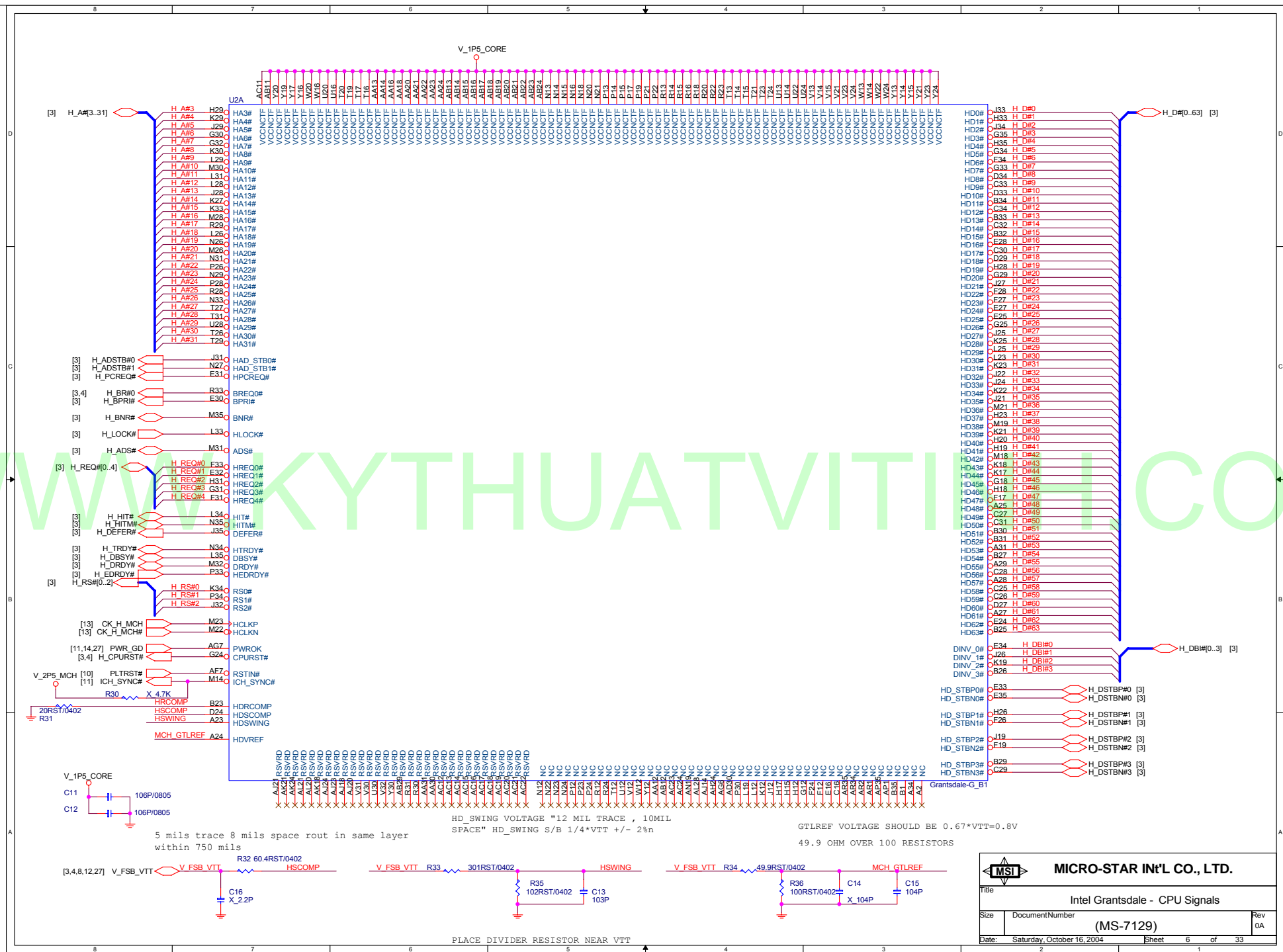
MS-7129 IBM Wellfleet Next Generation

System Block Diagram









[20] M_CHA_DQ[0..63]

[20,22] M_CHA_CKE[0..1]

[20] M_CHA_DM[0..7]

[20,22] -M_CHA_CS[0..1]

[20,22] -M_CHA_RAS
[20,22] -M_CHA_CAS
[20,22] -M_CHA_WE

[20,22] M_CHA_MA[0..13]

[20,22] M_CHA_ODT[0..1]

[20,22] M_CHA_BA[0..2]

[20] M_CHA_DQS0
[20] -M_CHA_DQS0
[20] M_CHA_DQS1
[20] -M_CHA_DQS1
[20] M_CHA_DQS2
[20] -M_CHA_DQS2
[20] M_CHA_DQS3
[20] -M_CHA_DQS3
[20] M_CHA_DQS4
[20] -M_CHA_DQS4
[20] M_CHA_DQS5
[20] -M_CHA_DQS5
[20] M_CHA_DQS6
[20] -M_CHA_DQS6
[20] M_CHA_DQS7
[20] -M_CHA_DQS7

[20] M_CHA_SCK0
[20] -M_CHA_SCK0
[20] M_CHA_SCK1
[20] -M_CHA_SCK1
[20] M_CHA_SCK2
[20] -M_CHA_SCK2

TP_SA RCVENOUT#
TP_SA RCVENIN
BUFFER SLEW A

SM_VREF
SM_RCOMP_P
SM_RCOMP_N
SMOCDCCMP1
SMOCDCCMP0

[21] M_CHB_DQ[0..63]

[21,22] M_CHB_CKE[0..1]

[21] M_CHB_DM[0..7]

-M_CHB_CS0
-M_CHB_CS1

-M_CHB_RAS
-M_CHB_CAS
-M_CHB_WE

M_CHB_MA0
M_CHB_MA1
M_CHB_MA2
M_CHB_MA3
M_CHB_MA4
M_CHB_MA5
M_CHB_MA6
M_CHB_MA7
M_CHB_MA8
M_CHB_MA9
M_CHB_MA10
M_CHB_MA11
M_CHB_MA12
M_CHB_MA13

M_CHB_ODT0
M_CHB_ODT1

M_CHB_BA0
M_CHB_BA1
M_CHB_BA2

M_CHB_DQS0
-M_CHB_DQS0
M_CHB_DQS1
-M_CHB_DQS1
M_CHB_DQS2
-M_CHB_DQS2
M_CHB_DQS3
-M_CHB_DQS3
M_CHB_DQS4
-M_CHB_DQS4
M_CHB_DQS5
-M_CHB_DQS5
M_CHB_DQS6
-M_CHB_DQS6
M_CHB_DQS7
-M_CHB_DQS7

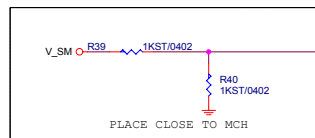
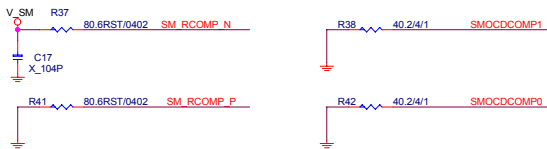
M_CHB_SCK0
-M_CHB_SCK0
M_CHB_SCK1
-M_CHB_SCK1
M_CHB_SCK2
-M_CHB_SCK2

TP_SB RCVENOUT
TP_SB RCVENIN
SMYSLEWIN
SMYSLEWOUT

SM_VREF
SMOCDCCMP1
SMOCDCCMP0

CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU

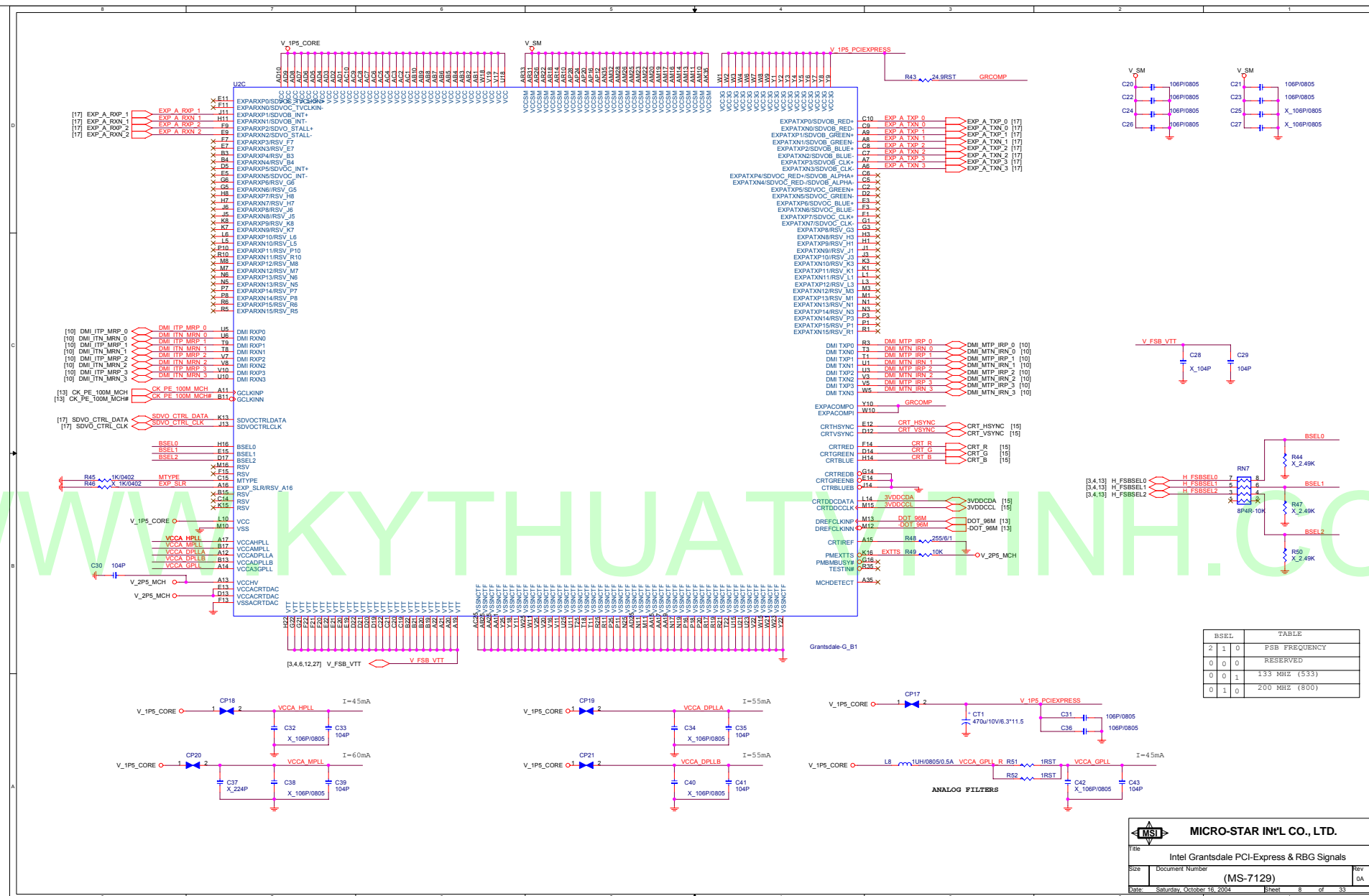


PLACE 0.1UF CAP CLOSE TO MCH




MICRO-STAR INT'L CO., LTD.

Title			Intel Grantsdale - Memory Signals		
Size			Document Number	Rev	0A
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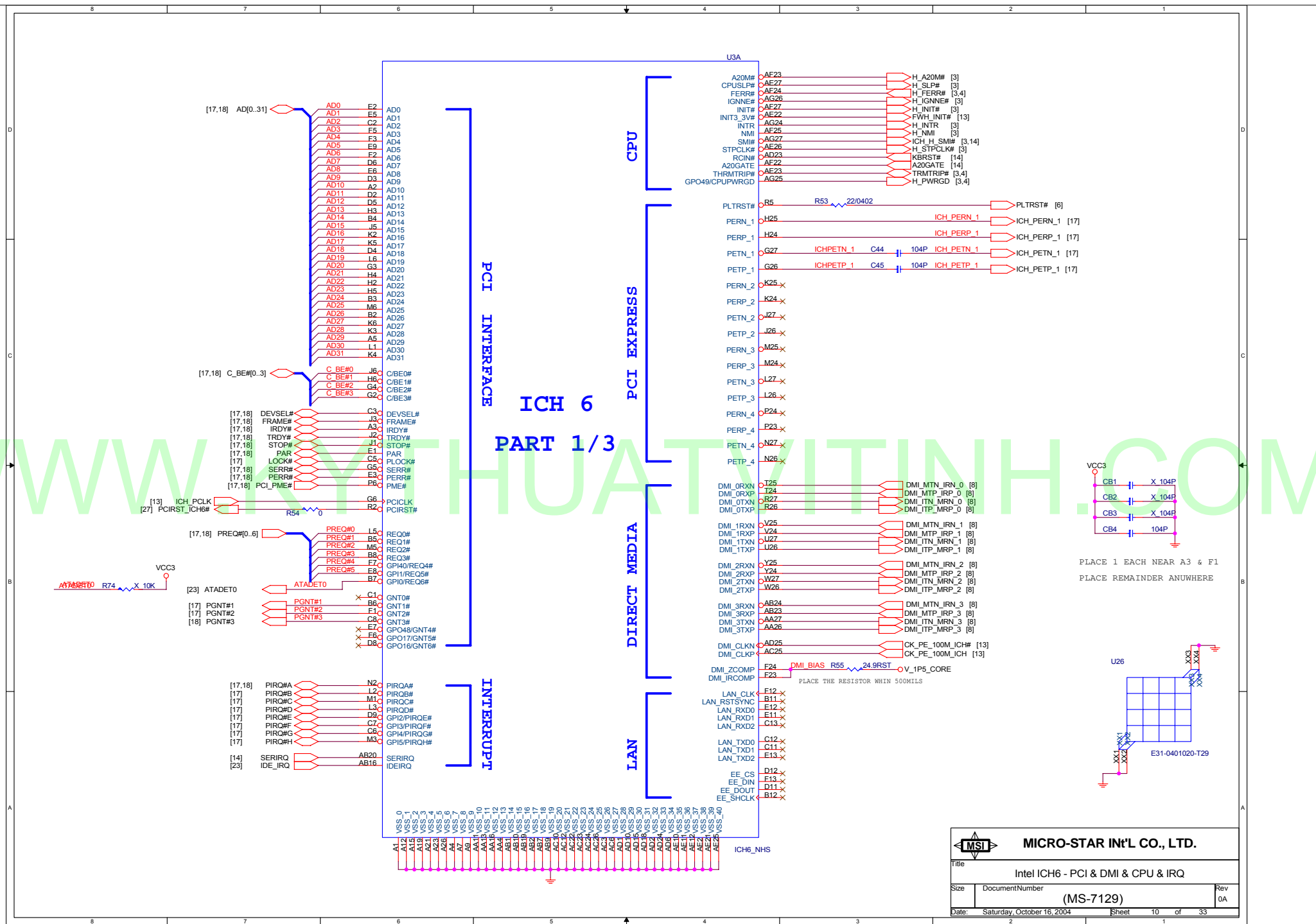
**MICRO-STAR INT'L CO., LTD.**

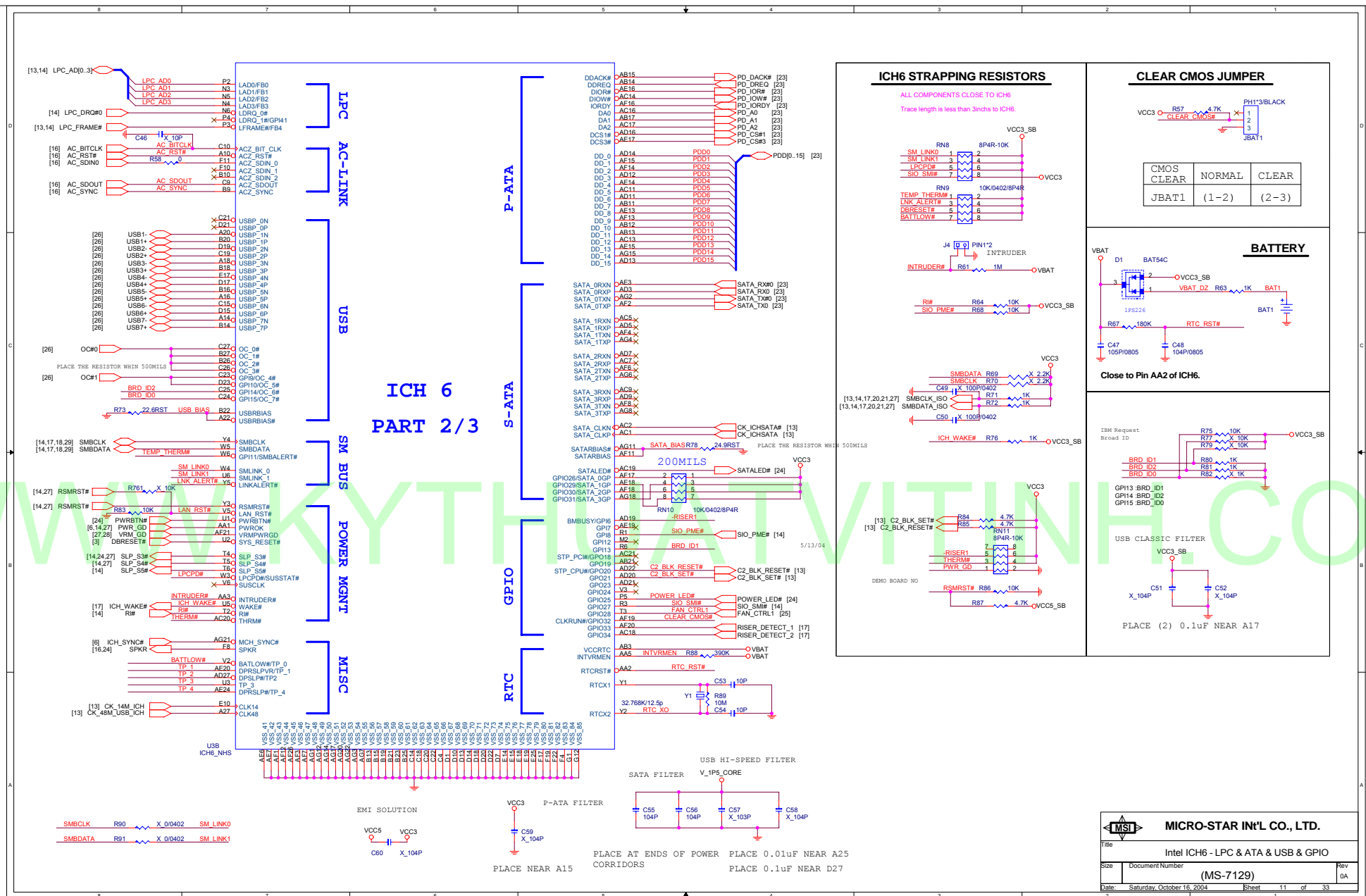
TitleIntel Grantsdale - GND

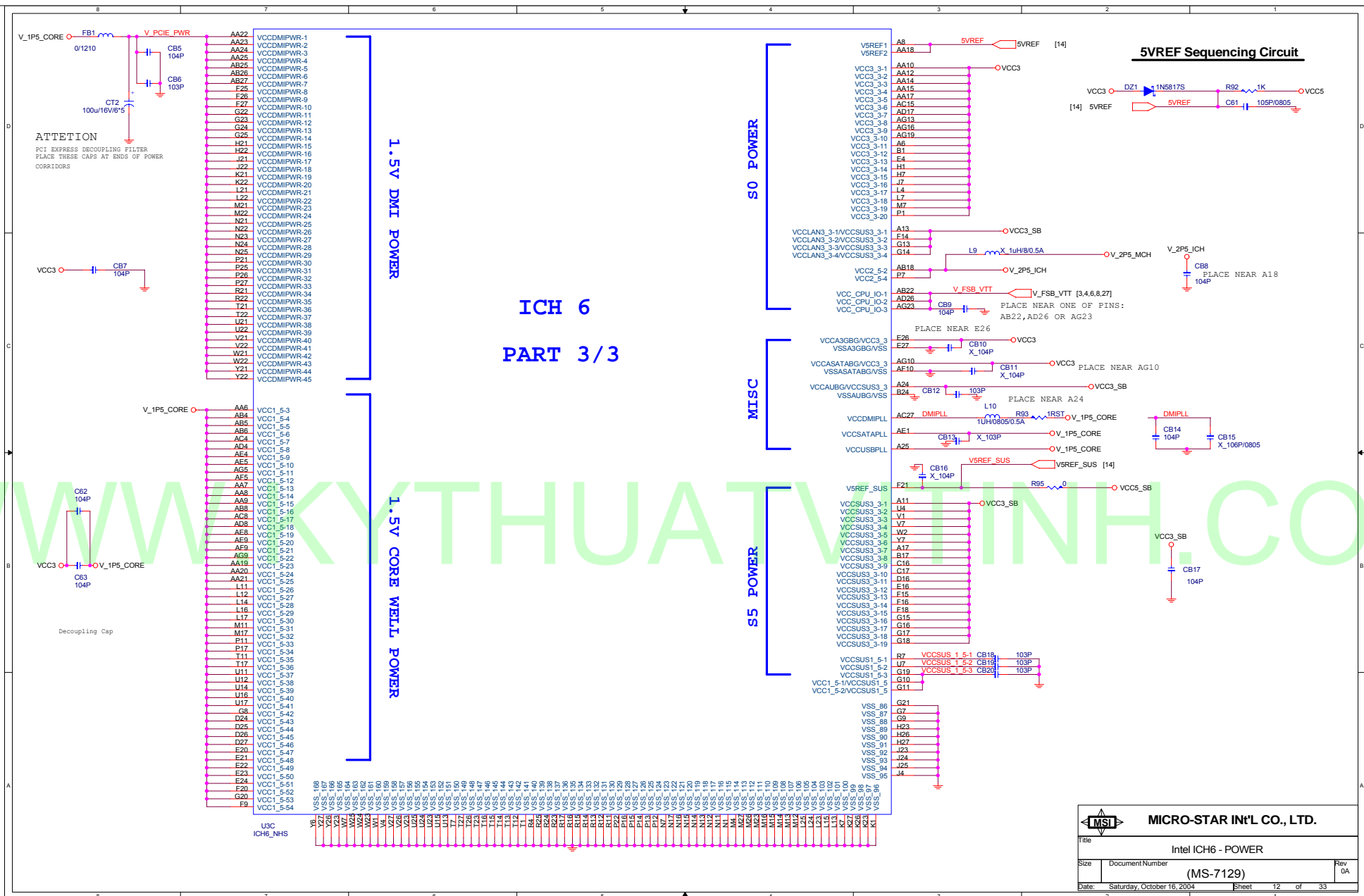
SizeDocumentNumberRevDA

(MS-7129)

Date: Saturday, October 16, 2004Sheet 9 of 33

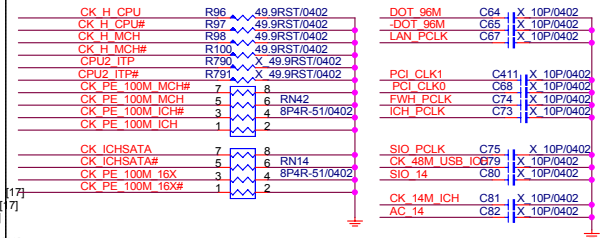
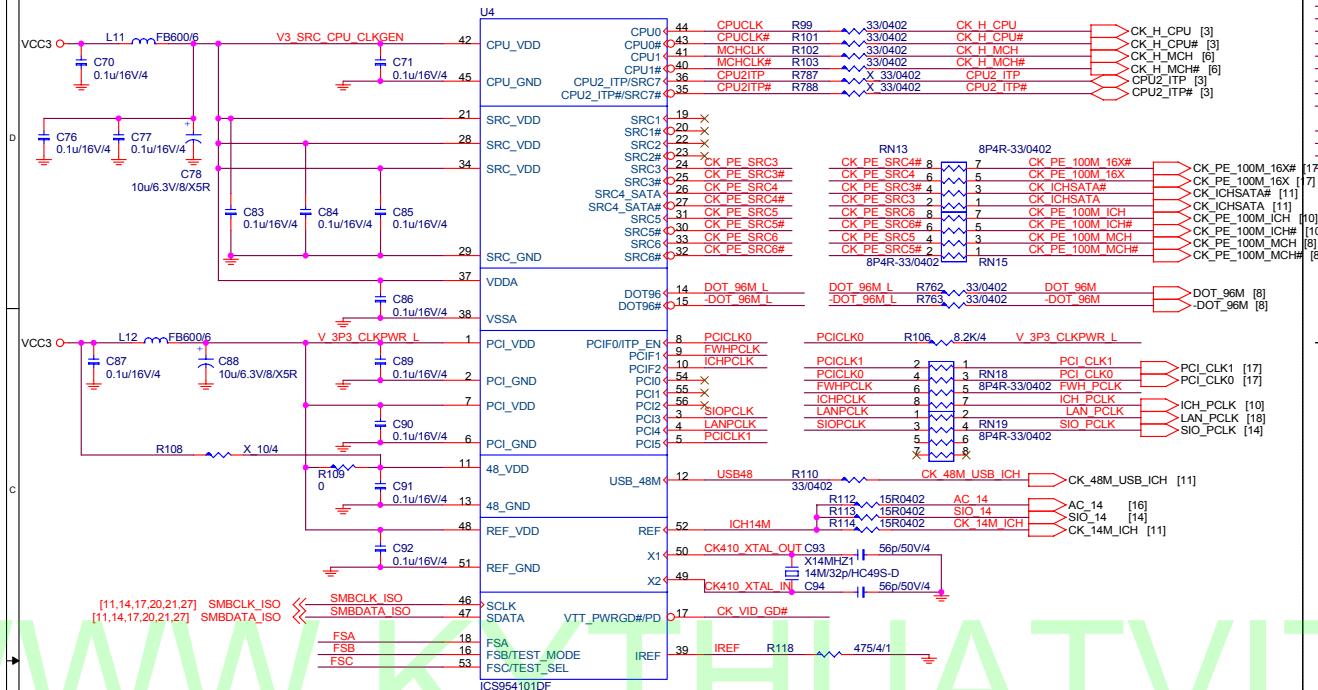






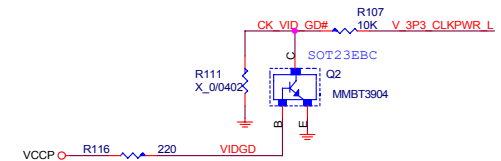
Clock Generator - ICS954101

Trace length less than 0.5inches

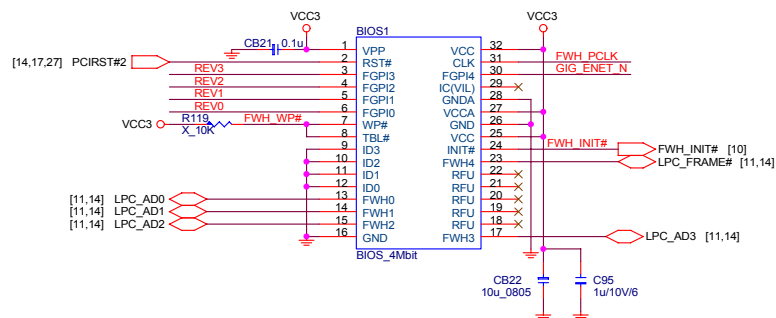


EMC HF filter capacitors, located close to PLL

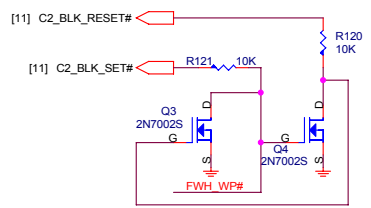
CLOCK GENERATOR VTT POWER DOWN BLOCK



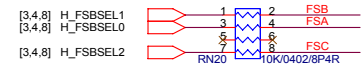
FIRMWARE HUB (FWH)



FWH WRITE PROTECT CIRCUIT

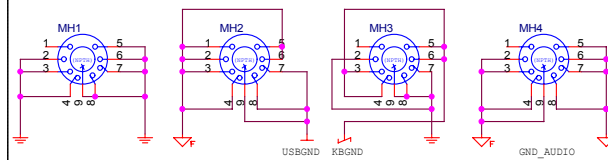


BSEL[0..2] Level Shift

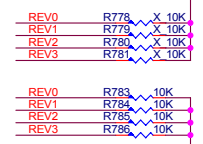


H_FSB_SEL				
2	1	0	CPU	
0	0	1	133	
0	1	0	200	

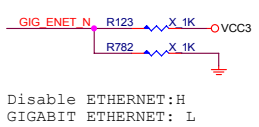
Mounting Holes



PCB REVISION ID



ETHERNET STRAPPING RESISTORS



MSI MICRO-STAR INT'L CO., LTD.

Title: CY28405 & FWH

Size: DocumentNumber: (MS-7129) Rev 0A

Date: Saturday, October 16, 2004 Sheet 13 of 33

LPC BUS SIGNALS

Pin connections for LPC1114 to LPC bus signals:

- Pin 13: SIO_PCLK
- Pin 11: LPC_FRAMER#
- Pin 1: LPC_DRQW#
- Pin 63: PCL_RESET
- Pin 13: PCIRSTW2
- Pin 17: PCIRST1
- Pin 2: PCIRST2
- Pin 55: PCL_CLK
- Pin 56: LFRAME
- Pin 57: LDRQ
- Pin 52: SMI
- Pin 53: SER_IRQ
- Pin 54: IO_SMM#
- Pin 51: IO_SMMW#
- Pin 50: ICH_H_SMM# [3:0]
- Pin 49: SERRQO [10]
- Pin 48: LPC_AD0
- Pin 47: LPC_AD1
- Pin 46: LPC_AD2
- Pin 45: LPC_AD3
- Pin 44: LPC_AD0..3 [1:13]

	27	RST#			
	30	DC0#			
	31	DTR, BOUT#	BADDR/XOR		
	32	RTS#/TRIS			
	27	TEST/TEST			
RSTB#	51	STB, WRITE			
RAFD#	50	AFD, DSTRB			
RINT#	48	INT			
RSUN#	47	SUN, ASTRB			
ERR#	46	ERR			
RACK#	36	ACK			
RBUSY	30	BUSY, WAIT			
RPE	30	PE			
RSCLT	33	SLCT			

RBUSY	35	BUSY_WAIT
RPE	34	PE
RSLCY	33	SLCT
<hr/>		
X 22	DENSEL	FLOPPY DISK INTERFACE
X 21	DRATE0	
X 20	INDEX	
X 19	MTR0	
X 18	DR0	
X 17	DIR	
X 16	STEP	

GLUE Logic Functions

[illegible]

Pin configuration for the System Wake Up Controller (SWC):

- 67: PRIMARY HD
- 68: SECONDARY HD
- 69: SCSI
- 66: HD_LED
- 75: GPIO13
- 101: GPIO14/IOPA0
- 106: GPIO16
- 80: GPIO17
- 31: GPIO16/IOP31/IOPA1
- 5V: 5V

75	GPIOE13	System Wake Up control (SWC)
X 101	GPIOE14/IOPA0	
100	GPIOE16	
80	GPIOE17	
X 91	GPIOE15/CLOCK32/IOPA1	FAN Control Monitoring
111	GPIOE06/FANTACH1	
112	GPIOE07/FANTACH2	
104	GPIOE01/FANTACH3	
X 105	GPIOE02/FANTACH4	

GPIO15/CLOCK32/IOPA1
GPIOE06/FANTACH1
GPIOE07/FANTACH2
GPIOE1/FANTACH3
GPIOE2/FANTACH4
NC/TPM_PP/IOPA6

FAN Control Monitoring

- GPIO07/FANTACH2
- GPIO01/FANTACH3
- GPIO02/FANTACH4

Other Signals

- NC/TPM_PP/IOPA6
- GPO11/VsbStrap1

Other Signals

POWER &

5V

NC/TPM_PP/IOPA6

GPO11/VsbStrap1

GPO12/VsbStrap2

VDD3

VDD3

VDD3

VDD3

VDD3

6

31

49

60

CB27

0.1u

POWER & GND

[illegible]

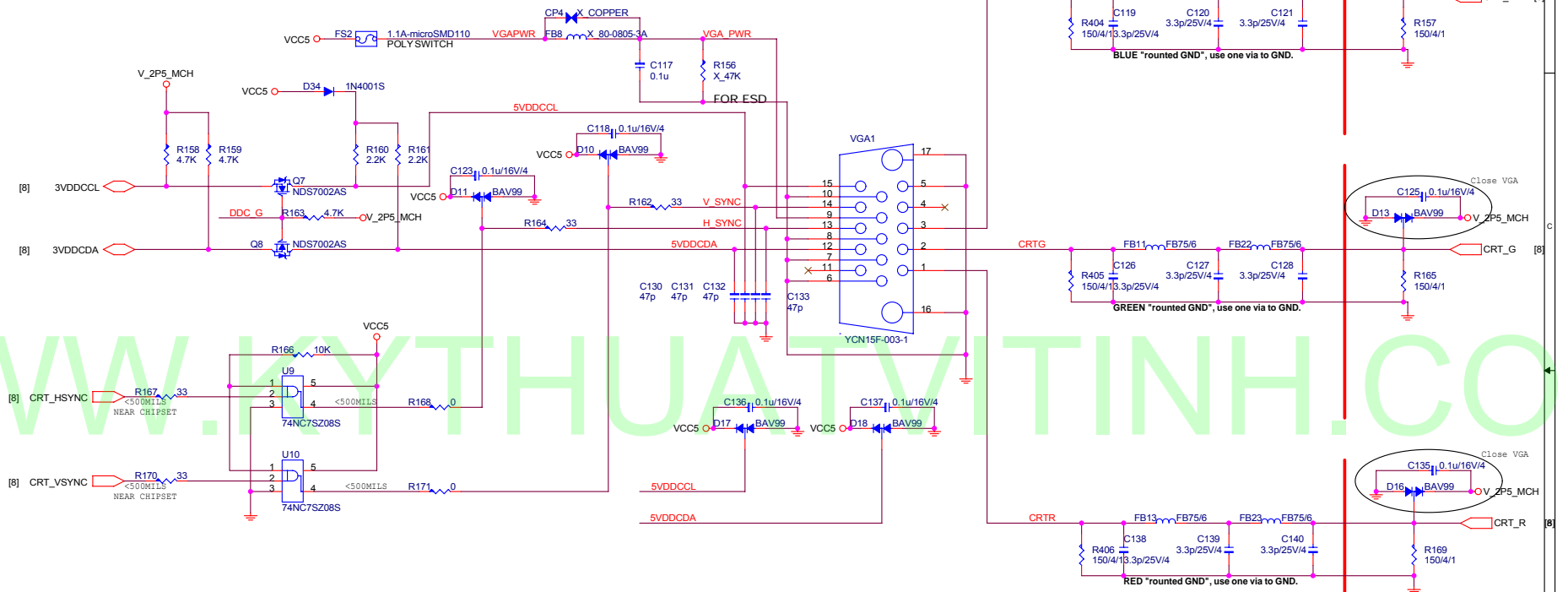
EMI FILTER
NOTES:

1.
PLACE CLOSE TO CONNECTORS
2.
CONNECT THE CAPACITORES TO SHIELD.
3.
ON THIS BOARD, DUE TO LAYOUT LIMITATIONS, THE CAPACITORS ARE CONNECTED TO GND.

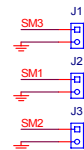
[illegible]

Title		NS PC8374L/K/T & I/O Conn.	
Size	Document Number	Rev	
	(MS-7129)	0A	
Date	Saturday, October 16, 2004	Sheet	14 of 33

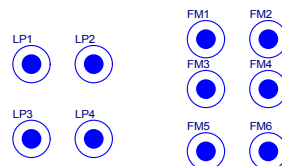
VIDEO CONNECTOR



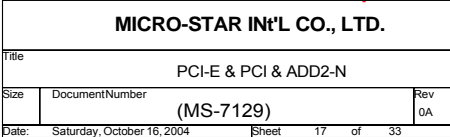
Simulation




Optics Orientation Holes



MICRO-STAR INT'L CO., LTD.			
Title: VGA CONNECTORS			
Size:	Document Number:	Rev: 0A	
Date: Saturday, October 16, 2004		Sheet: 15	of 33

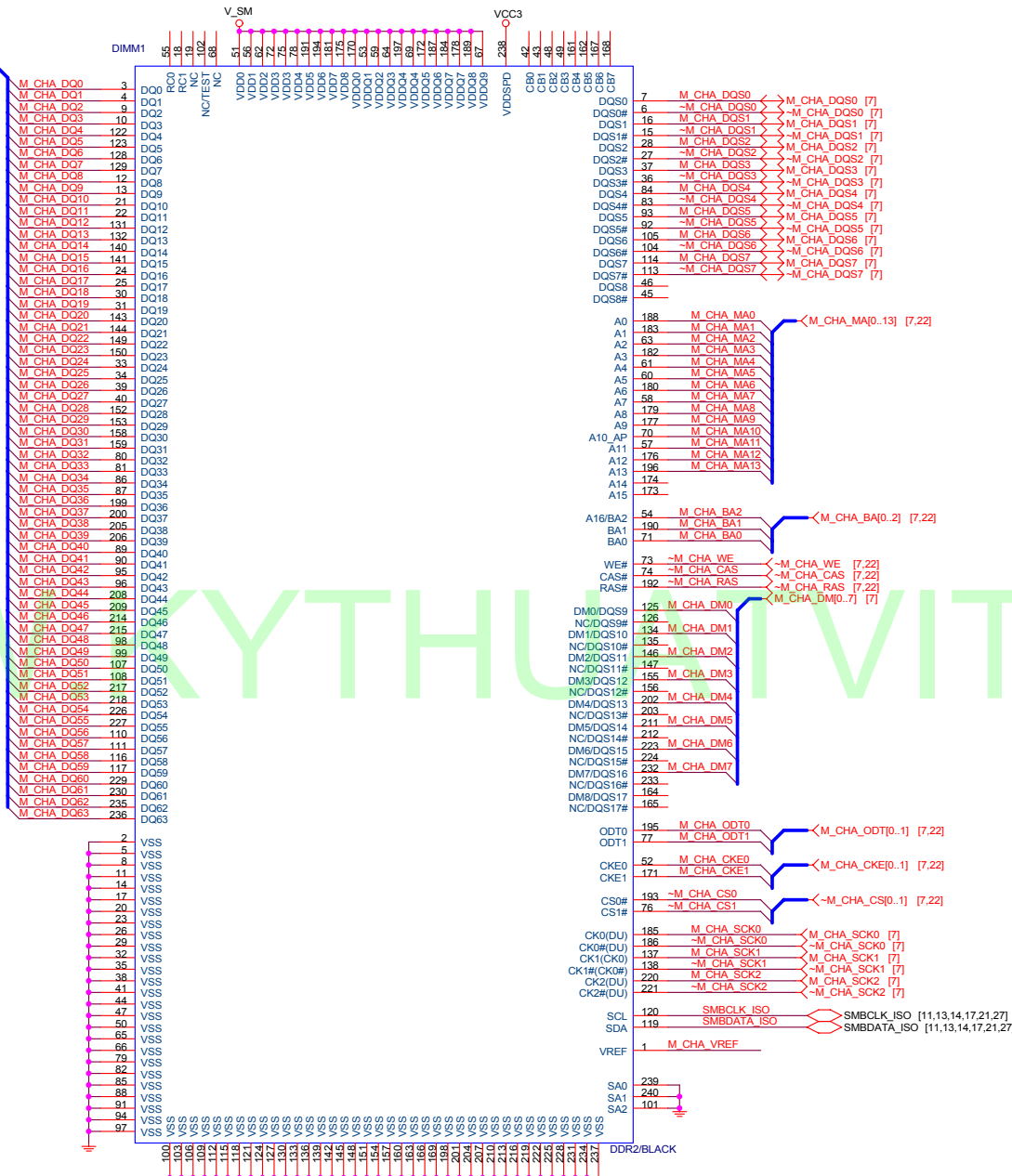


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Date:	Saturday, October 16, 2004		Sheet 19 of 33

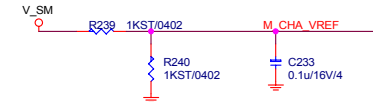
DDR2 DIMM1

[7] M_CHA_DQ[0..63] <--



ADDR.=1010000B(A0H)

PLACE 0.1UF CAP CLOSE TO RESISTOR DIVIDER

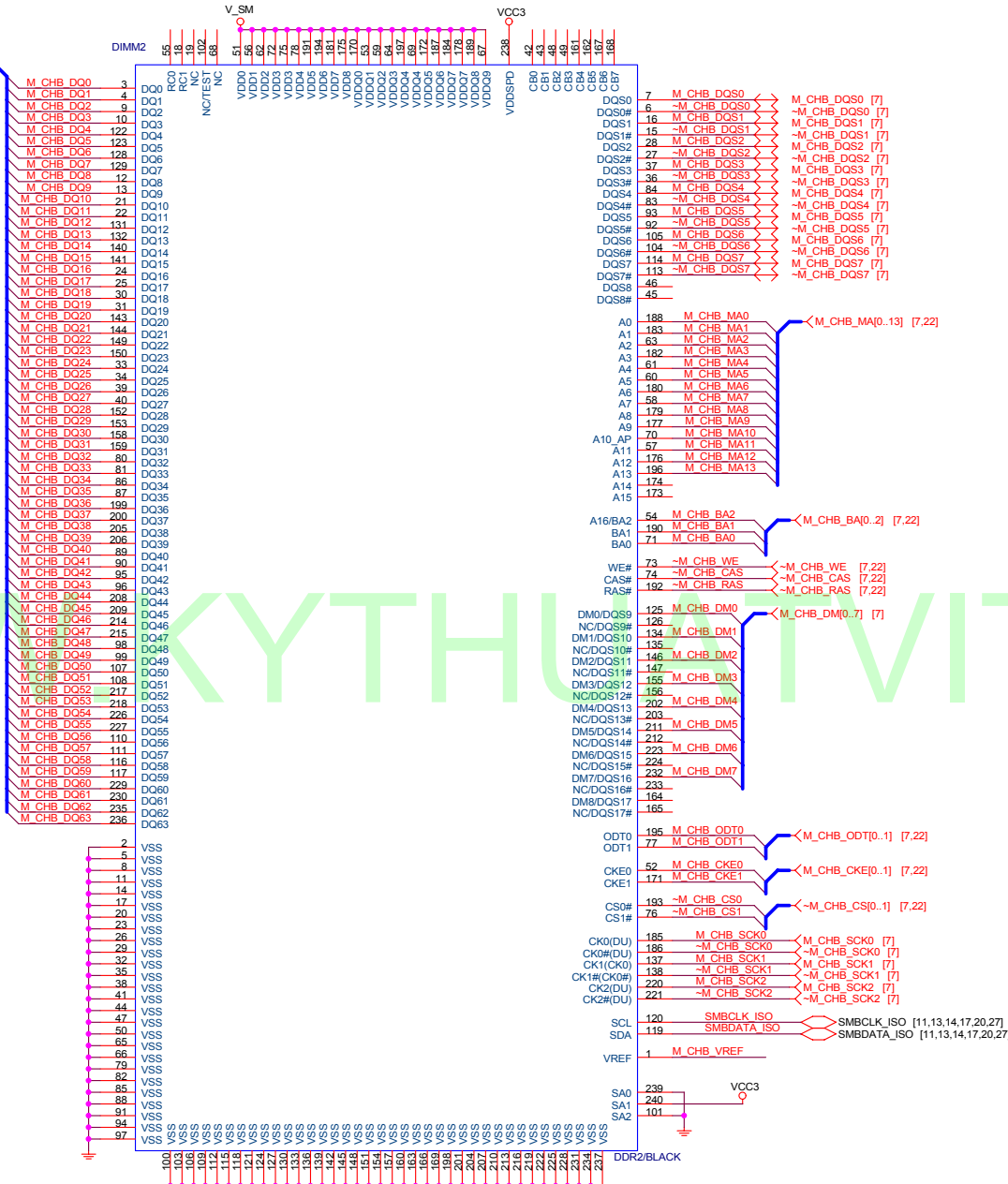


PLACE CLOSE TO CH_A DIMMS

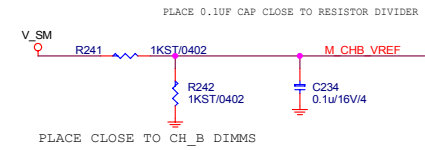
MICRO-STAR INT'L CO., LTD.		
Title DDR II DIMM 1		
Size	Document Number (MS-7129)	Rev 0A
Date	Saturday, October 16, 2004	Sheet 20 of 33

DDR2 DIMM2

[7] M_CHB_DQ[0..63] <--

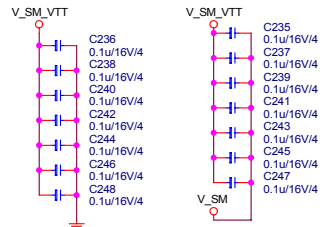


ADDR.=1010010B(A4H)



MICRO-STAR INT'L CO., LTD.		
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Size:	Document Number:	Rev: 0A
Date: Saturday, October 16, 2004		Sheet: 21 of 33

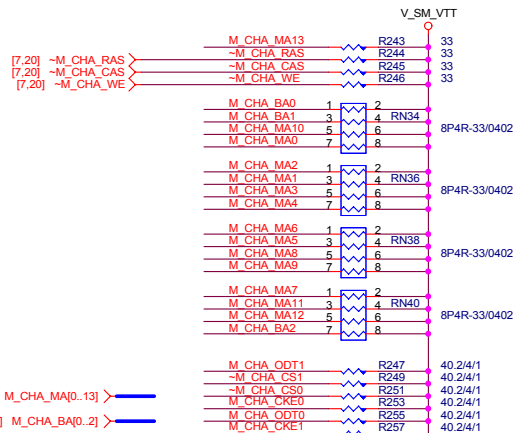
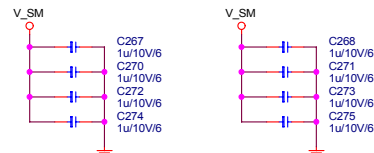
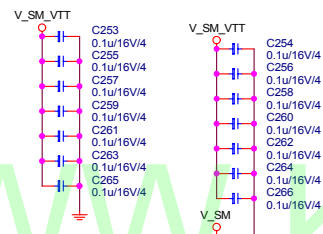
CH A +0.9V DECOUPLING CAPS



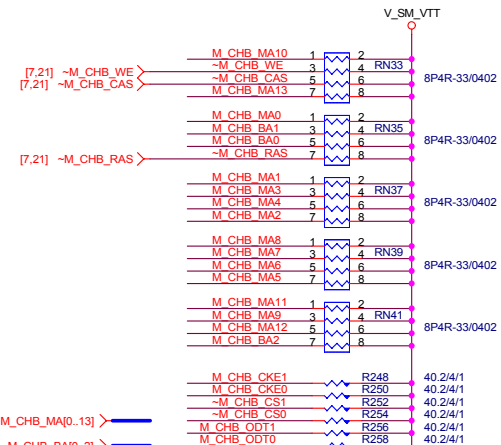
PLACED AT LEFT AND RIGHT ENDS OF VTT ISLAND



CH B +0.9V DECOUPLING CAPS

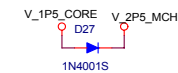
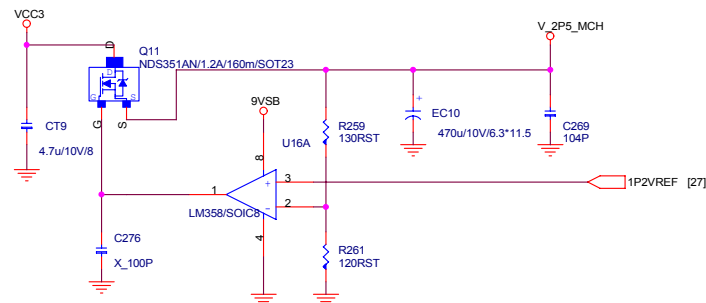


[7.20] M_CHA_MA[0..13] >
[7.20] M_CHA_BA[0..2] >
[7.20] M_CHA_CS[0..1] >
[7.20] M_CHA_CKE[0..1] >
[7.20] M_CHA_ODT[0..1] >



[7.21] M_CHB_WE >
[7.21] M_CHB_CAS >
[7.21] M_CHB_RAS >
[7.21] M_CHB_MA[0..13] >
[7.21] M_CHB_BA[0..2] >
[7.21] M_CHB_CS[0..1] >
[7.21] M_CHB_CKE[0..1] >
[7.21] M_CHB_ODT[0..1] >

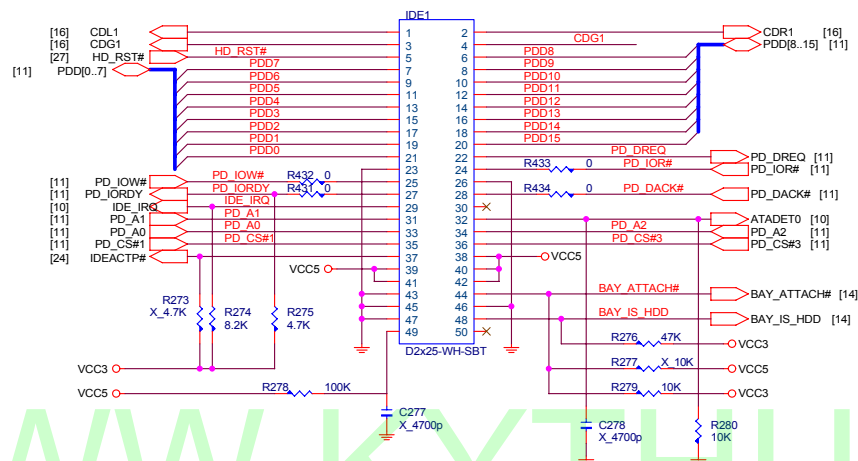
Grantsdale GMCH Power Sequencing Requirement Between 1.5V Core and 2.5V DAC



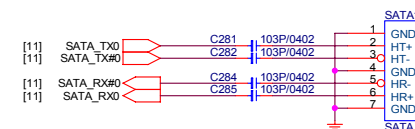
MICRO-STAR INT'L CO., LTD.		
Title: DDR 2 VTT DECOUPLING		
Size:	Document Number:	Rev: 0A
Date: Saturday, October 16, 2004		
Sheet: 22 of 33		

PRIMARY SLIME IDE

IBM Ultrabay Slim and Ultrabay Enhanced



SERIAL ATA CONNECTOR BLOCK

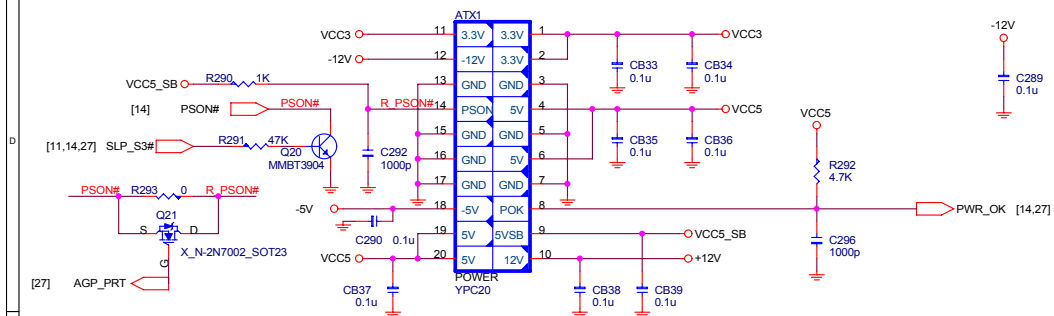


Default 10nF ,
Option 0 ohm

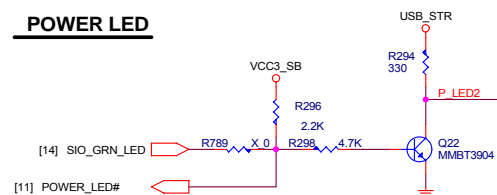
20:5:7:5:20<5"

MICRO-STAR INT'L CO., LTD.			
Title IBM Slim IDE & SATA CONN.			
Size	DocumentNumber (MS-7129)		Rev 0A
Date:	Saturday, October 16, 2004	Sheet	23 of 33

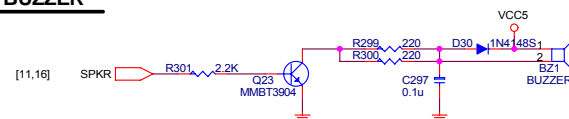
ATX CONNECTOR



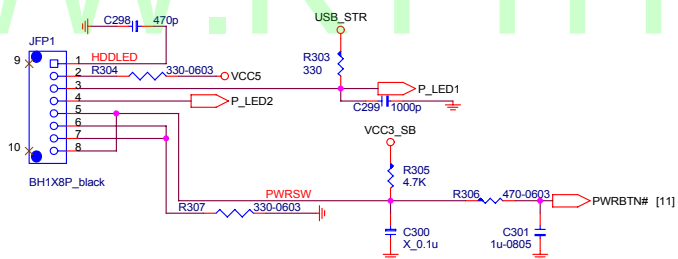
POWER LED



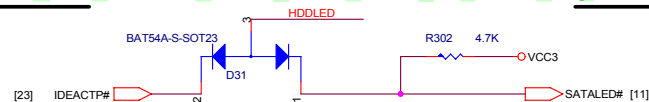
BUZZER



FRONT PANEL



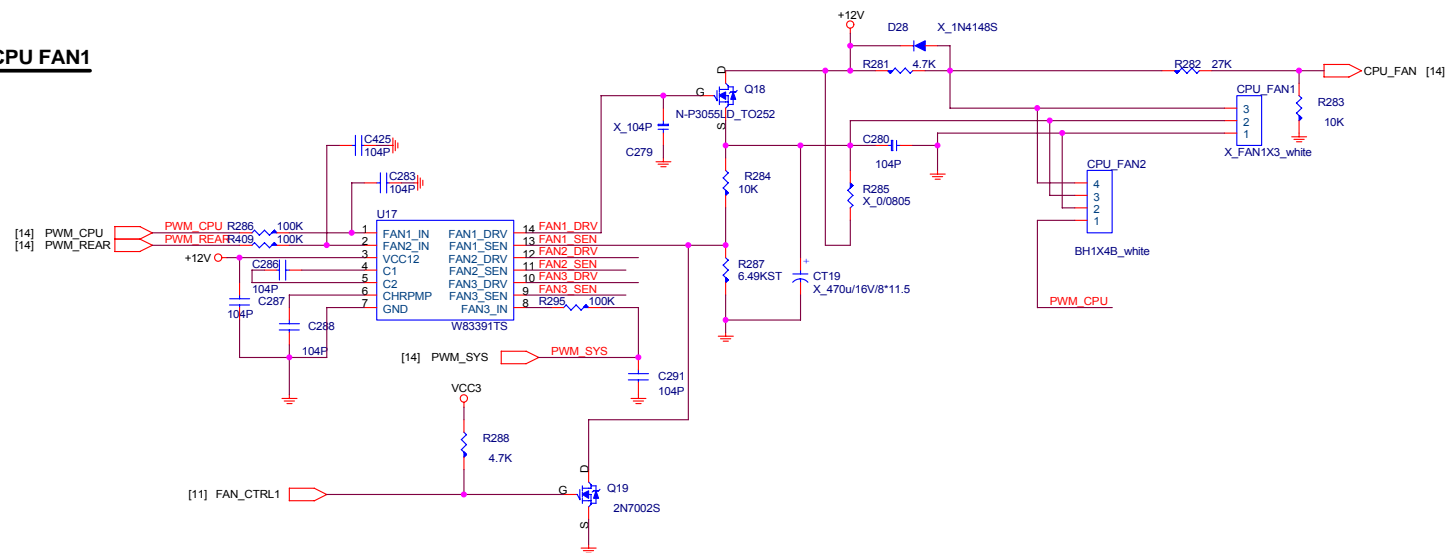
IDE LED



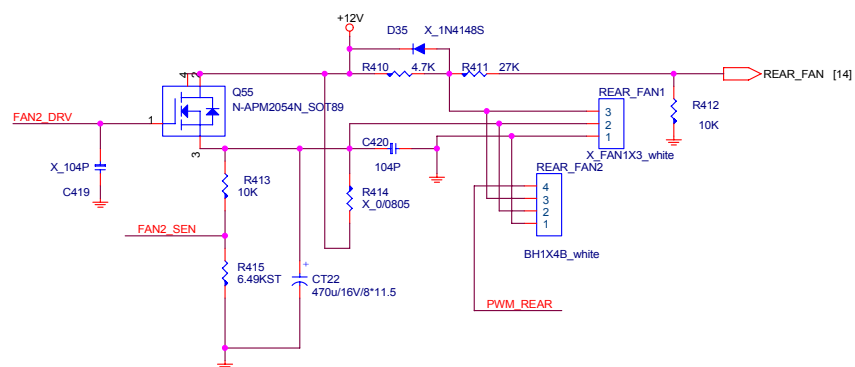
SATA LED

MICRO-STAR INT'L CO., LTD.			
Title: ATX & FRONT PANEL			
Size:	DocumentNumber:	Rev: 0A	
Date: Saturday, October 16, 2004		Sheet: 24 of 33	

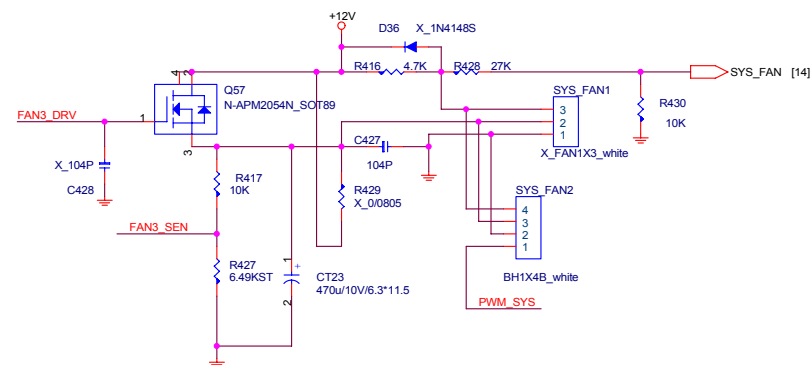
CPU FAN1



REAR FAN1



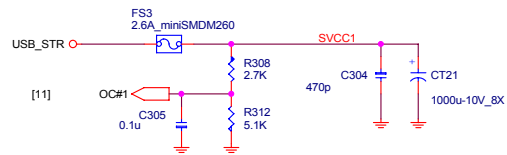
SYSTEM FAN1



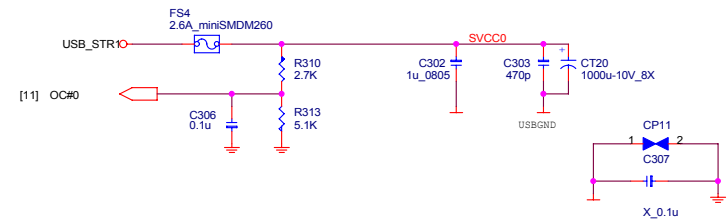
MICRO-STAR INT'L CO., LTD.

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Size	Document Number	Rev	
	(MS-7129)	0A	
Date:	Saturday, October 16, 2004	Sheet	25 of 33

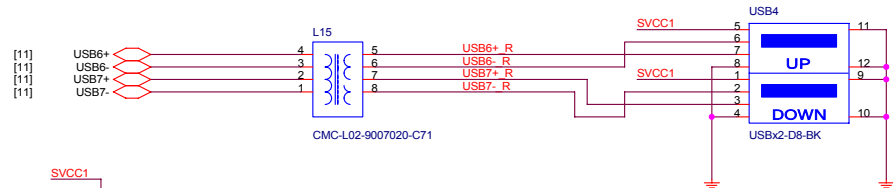
POWER CIRCUIT FOR USB PORT 4,5,6,7



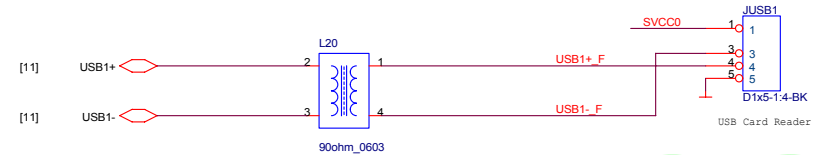
POWER CIRCUIT FOR USB PORT 0,1,2,3



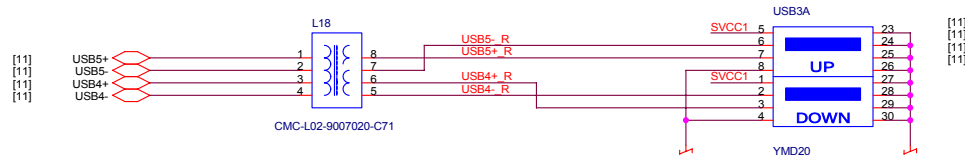
REAR PANEL USB CONNECTOR FOR USB PORT 6,7



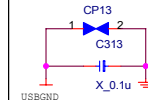
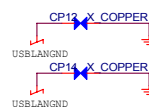
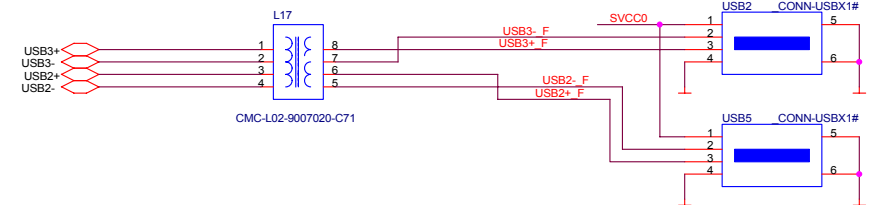
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



REAR PANEL USB CONNECTOR FOR USB PORT 4,5



FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



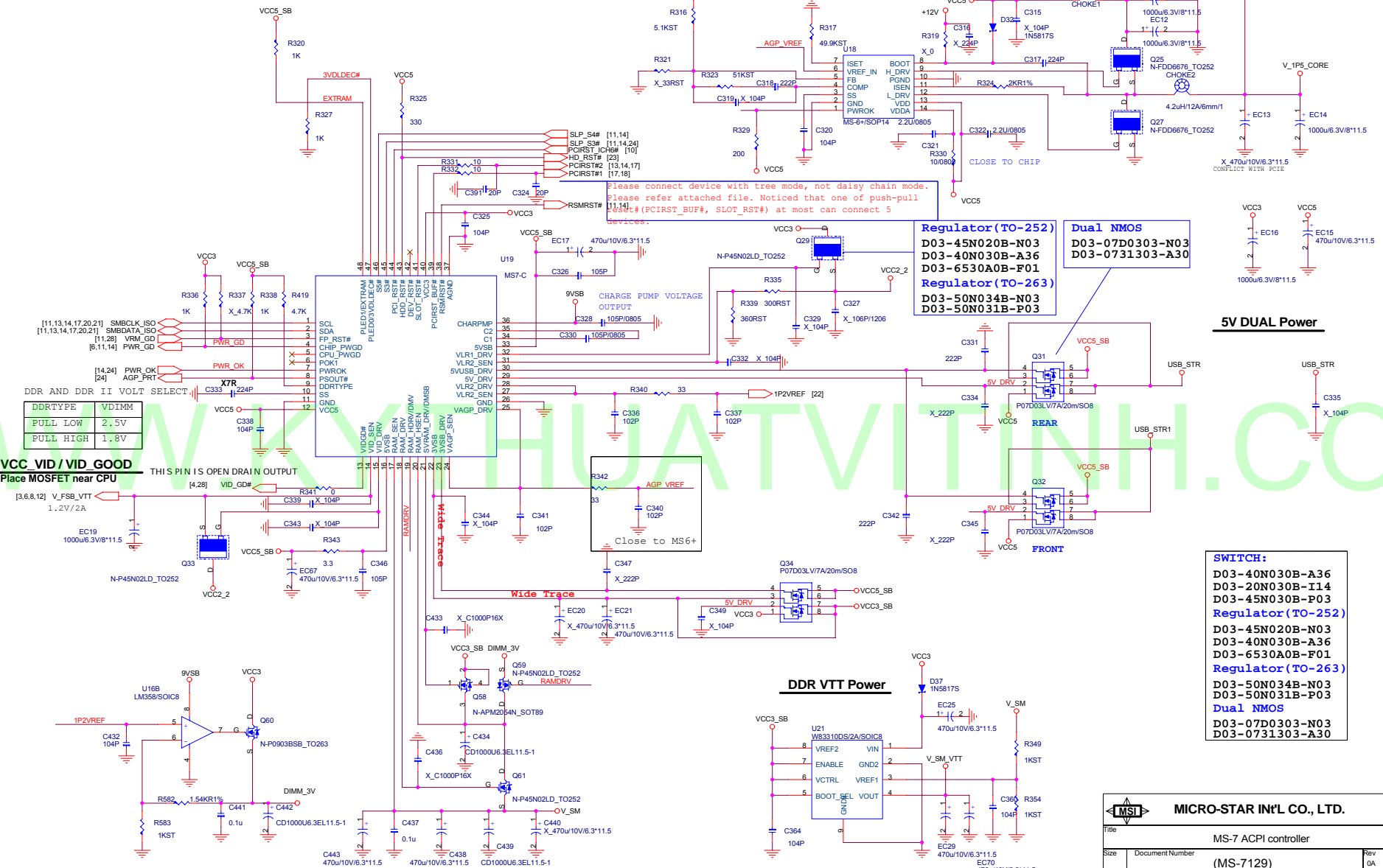
MICRO-STAR INT'L CO., LTD.			
Title USB Connectors			
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ACPI Controller

3VSB MODE SELECT VDIMM LINEAR OR PWM SELECT

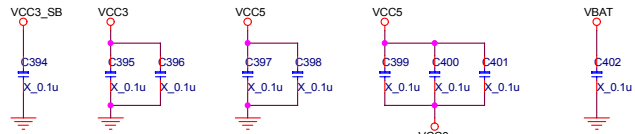
3VSB MODE	3VSB MODE SELECT	VDIMM MODE	EXTRAM
SINGLE MOSFET	PULL HIGH	LINEAR REGULATOR	PULL LOW
DUAL MOSFET	PULL LOW	PWM REGULATOR	PULL HIGH

MCH CORE POWER



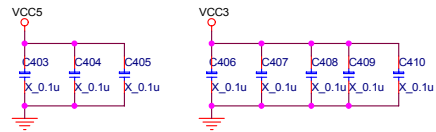
SWITCH:
D03-40N030B-A36
D03-20N030B-I14
D03-45N030B-P03
Regulator (TO-252)
D03-45N020B-N03
D03-40N030B-A36
D03-6530A0B-F01
Regulator (TO-263)
D03-50N034B-N03
D03-50N031B-P03
Dual NMOS
D03-07D0303-N03
D03-0731303-A30


EMI Decoupling CAP



Vcc3 & Vcc5 Bridge

Decoupling CAP



 MICRO-STAR INT'L CO., LTD.	
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ICH6

GPIO Pin	Type	Function
GPIO 0	I	ATADET0
GPIO 1	I	PREQ5# (multifunction pin)
GPIO 2	I	PIRQ#E (multifunction pin)
GPIO 3	I	PIRQ#F (multifunction pin)
GPIO 4	I	PIRQ#G (multifunction pin)
GPIO 5	I	PIRQ#H (multifunction pin)
GPIO 6	I	-RISER1 (multifunction pin)
GPIO 7	I	Unused
GPIO 8	I	SIO_PME#
GPIO 9	I	Unused/OC_4# (multifunction pin)
GPIO 10	I	Unused/OC_5# (multifunction pin)
GPIO 11	I	Unused/SMBAlert# (multifunction pin)
GPIO 12	I	Unused
GPIO 13	I	BRD_ID1
GPIO 14	I	BRD_ID2/OC_6#(multifunction pin)
GPIO 15	I	BRD_ID0/OC_7#(multifunction pin)
GPIO 16	O	PGNT6# (multifunction pin)
GPIO 17	O	PGNT5# (multifunction pin)
GPIO 18	O	Unused
GPIO 19	O	Unused
GPIO 20	O	C2_BLK_RESET# (multifunction pin)
GPIO 21	O	C2_BLK_SET# (multifunction pin)
GPIO 22	OD	Unused (multifunction pin)
GPIO 23	O	Unused
GPIO 24	I/O	Unused
GPIO 25	I/O	ICH_POWER_LED#
GPIO 27	I/O	SIO_SMI# (multifunction pin)
GPIO 28	I/O	FAN_CTR1
GPIO 32	I/O	CLEAR_CMOS#
GPIO 33	I/O	Riser_DETECT_1 (A1)
GPIO 34	I/O	Riser_DETECT_2 (A48)
GPIO 40	I	PREQ#4 (multifunction pin)
GPIO 41	I	LDRQ1 (multifunction pin)
GPIO 48	O	PGNT#4 (multifunction pin)
GPIO 49	OD	H_PWRGD (multifunction pin)

Flash ROM(PCB REVISION ID)

GPIO Pin	Type	OA			
GPI 0	I	0			
GPI 1	I	0			
GPI 2	I	0			
GPI 3	I	0			
GPI 4	I	NC			

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Riser Slot	PIRQ#E	PREQ#1	AD28	PCICLK1	Pin-56
	PIRQ#F	PGNT#1		PCICLK2	Pin-4
	PIRQ#G	PREQ#2			
	PIRQ#H	PGNT#2			
LAN BCM5705	PIRQ#A	PREQ#3	AD27	LAN_PCLK	Pin-55

LPC SIO NS PC8374L/K/T

GPIO Pin	Type	Pin	Function
GPIOE 00	I/O	103	PORTBOTH-R
GPIOE 01	I/O	104	SYS_FAN
GPIOE 02	I/O	105	Unused
GPIOE 03	I/O	106	PWM_CPU
GPIOE 04	I/O	108	PWM_REAR
GPIOE 05	I/O	109	PWM_SYS
GPIOE 06	I/O	111	CPU_FAN
GPIOE 07	I/O	112	REAR_FAN
GPIOE 00	I/O	118	Unused/IRTX
GPIOE 01	I/O	119	RI2#/SIN2
GPIOE 02	I/O	120	Unused/IRRX
GPIOE 03	I/O	121	DSR2/SIN2#
GPIOE 04	I/O	124	DSR2#/CTS2#
GPIOE 05	I/O	126	CTS2/DCD2#/DSR2#
GPIOE 06	I/O	127	DTR_BOUT2#/IRRX
GPIOE 07	I/O	128	DCD2#/IRTX
GPIOE 10	I/O	116	Unused/5V_DDCSDA
GPIOE 11	I/O	114	Unused/5V_DDCSCL
GPIOE 12	I/O	115	Unused/CC_DDCSDA
GPIOE 13	I/O	113	Unused/CC_DDCSCL
GPIOE 12	I/O	74	Unused/PCIRST_OUT2#
GPIOE 13	I/O	75	Unused/TAMPER
GPIOE 14	I/O	101	Unused/IOPA0
GPIOE 16	I/O	100	BAY_ATTACH#
GPIOE 17	I/O	80	BAY_IS_HDD
GPIO 11	O	117	Unused/FLOCK#
GPIO 12	O	91	Unused/IOPA1/CLOCKI32
GPIO 13	O	122	SOUT2#/RTS2#
GPIO 15	O	125	RTS2#/DTR_BOUT2#

DDR DIMM Config.


DEVICE	ADDRESS	CLOCK
DIMM 1	AOH	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A4H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2

PCI RESET DEVICE

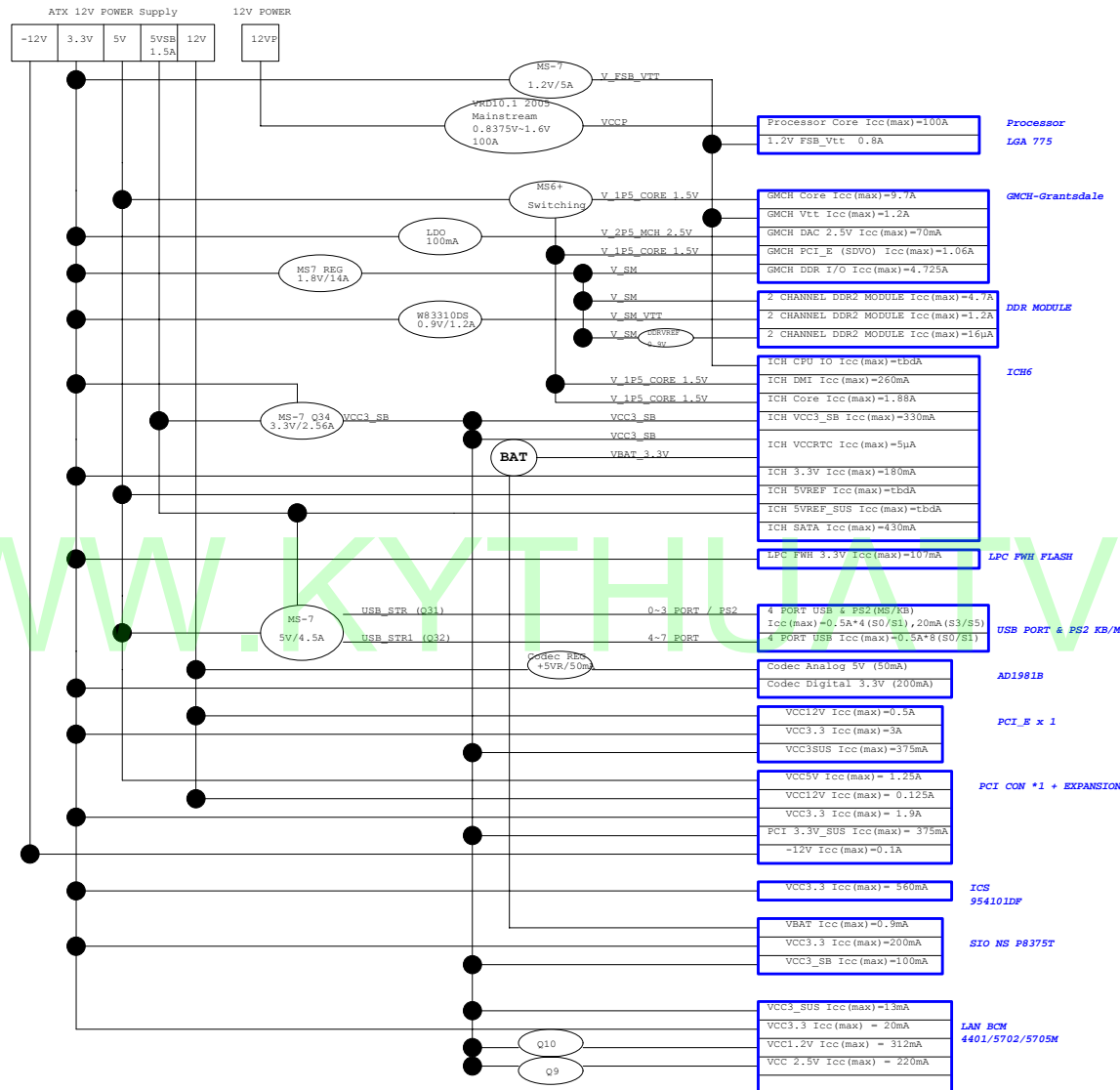
Signals	Target
PCIRST#1	PCI-E Slot, LAN
PCIRST#2	Super I/O, FWH, PCI-E
PCIRST_ICH6#	Northbridge , MS-7
HDDRST#	Primary IDE

JUMPER SETTING

JBAT1	(1-2) NORMAL	(2-3) CLEAR
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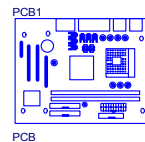
 MICRO-STAR INT'L CO., LTD.	
Title General Purpose Spec & JUMPER SETTING	
Size Document Number	Rev 0A
(MS-7129)	
Date: Saturday, October 16, 2004	Sheet 30 of 33

POWER DELIVERY MAP



VRM SPEC	Transition	Sustain	Power Consumption
VRM9.0 mPG 478	FMB1.0	60A	50A
	FMB2.0	70A	60A
VRM10.0 mPG 478	FMB1.0	78A	68A
	FMB1.5	91A	81A
	2004 Performance	119A	101A
VRM10.1 LGA 775	2004 Mainstream	78A	68A
	2005 Performance	125A	115A
	2005 Mainstream	100A	85A
			95W/XX

Manual Parts



MODEL Config.	ORCAD Config.	Function	Option	ERP Number	

 MICRO-STAR INT'L CO., LTD.	
Title: Manual Parts & decoupling	
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